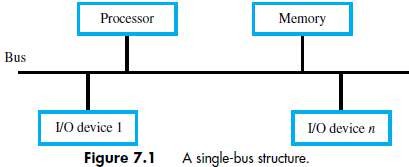
**MODULE 3: INPUT/OUTPUT ORGANIZATION**

# ACCESSING I/O-DEVICES

* A **single bus-structure** can be used for connecting I/O-devices to a computer (Figure 7.1).
* Each I/O device is assigned a unique set of address.
* Bus consists of 3 sets of lines to carry address, data & control signals.
* When processor places an address on address-lines, the intended-device responds to the command.
* The processor requests either a read or write-operation.
* The requested-data are transferred over the data-lines.



* There are 2 ways to deal with I/O-devices: 1) Memory-mapped I/O & 2) I/O-mapped I/O.

# Memory-Mapped I/O

* + Memory and I/O-devices share a common address-space.
  + Any data-transfer instruction (like Move, Load) can be used to exchange information.
  + For example,

*Move DATAIN, R0;* This instruction sends the contents of location DATAIN to register R0.

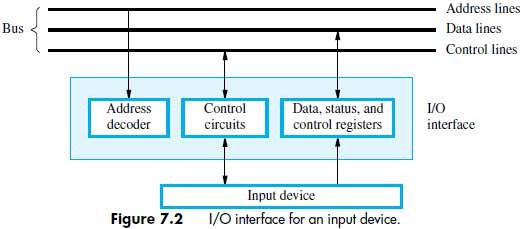
Here, DATAIN  address of the input-buffer of the keyboard.

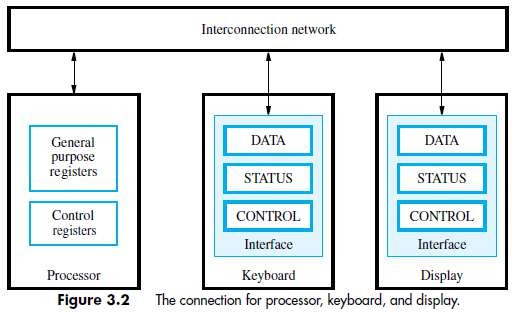
# I/O-Mapped I/O

* + Memory and I/0 address-spaces are different.
  + A special instructions named **IN** and **OUT** are used for data-transfer.
  + Advantage of separate I/O space: I/O-devices deal with fewer address-lines.

# I/O Interface for an Input Device

1. **Address Decoder:** enables the device to recognize its address when this address appears on the address-lines (Figure 7.2).
2. **Status Register:** contains information relevant to operation of I/O-device.
3. **Data Register:** holds data being transferred to or from processor. There are 2 types:
   1. DATAIN  Input-buffer associated with keyboard.
   2. DATAOUT  Output data buffer of a display/printer.





# MECHANISMS USED FOR INTERFACING I/O-DEVICES

1. **Program Controlled I/O**

* Processor repeatedly checks status-flag to achieve required synchronization b/w processor & I/O device. (We say that the processor polls the device).
* Main drawback:

The processor wastes time in checking status of device before actual data-transfer takes place.

# Interrupt I/O

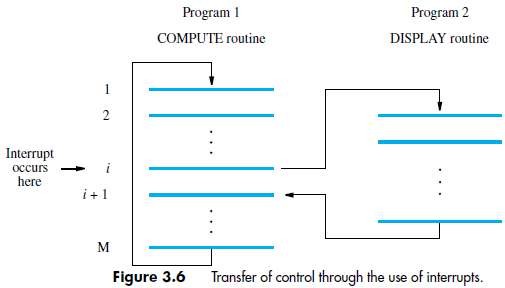
* I/O-device initiates the action instead of the processor.
* I/O-device sends an INTR signal over bus whenever it is ready for a data-transfer operation.
* Like this, required synchronization is done between processor & I/O device.

# Direct Memory Access (DMA)

* Device-interface transfer data directly to/from the memory w/o continuous involvement by the processor.
* DMA is a technique used for high speed I/O-device.

# INTERRUPTS

* There are many situations where other tasks can be performed while waiting for an I/O device to become ready.
* A hardware signal called an Interrupt will alert the processor when an I/O device becomes ready.
* Interrupt-signal is sent on the interrupt-request line.
* The processor can be performing its own task without the need to continuously check the I/O-device.
* The routine executed in response to an interrupt-request is called ISR.
* The processor must inform the device that its request has been recognized by sending INTA signal. (INTR  Interrupt Request, INTA  Interrupt Acknowledge, ISR  Interrupt Service Routine)
* For example, consider COMPUTE and PRINT routines (Figure 3.6).



* The processor first completes the execution of instruction i.
* Then, processor loads the PC with the address of the first instruction of the ISR.
* After the execution of ISR, the processor has to come back to instruction i+1.
* Therefore, when an interrupt occurs, the current content of PC is put in temporary storage location.
* A return at the end of ISR reloads the PC from that temporary storage location.
* This causes the execution to resume at instruction i+1.
* When processor is handling interrupts, it must inform device that its request has been recognized.
* This may be accomplished by INTA signal.
* The task of saving and restoring the information can be done automatically by the processor.
* The processor saves only the contents of **PC & Status register.**
* Saving registers also increases the Interrupt Latency.
* **Interrupt Latency** is a delay between

→ time an interrupt-request is received and

→ start of the execution of the ISR.

* Generally, the long interrupt latency in unacceptable.

# Difference between Subroutine & ISR

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Subroutine** | **ISR** | | | | | | |
| A subroutine performs a function required by the program from which it is called. | ISR may not have anything in common with program being executed at time INTR is received | | | | | | |
| Subroutine is just a linkage of 2 or more function  related to each other. | Interrupt  transfers. | is | a | mechanism | for | coordinating | I/O |

**INTERRUPT HARDWARE**

* Most computers have several I/O devices that can request an interrupt.
* A single interrupt-request (IR) line may be used to serve n devices (Figure 4.6).
* All devices are connected to IR line via switches to ground.
* To request an interrupt, a device closes its associated switch.
* Thus, if all IR signals are inactive, the voltage on the IR line will be equal to Vdd.
* When a device requests an interrupt, the voltage on the line drops to 0.
* This causes the INTR received by the processor to go to 1.
* The value of INTR is the logical OR of the requests from individual devices.

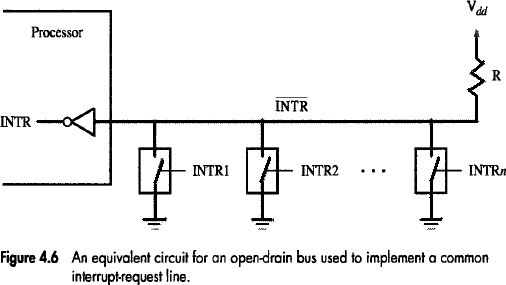
**INTR=INTR1+ INTR2+ +INTRn**

* A special gates known as open-collector or open-drain are used to drive the INTR line.
* The Output of the open collector control is equal to a switch to the ground that is

→ open when gates input is in ”0‟ state and

→ closed when the gates input is in “1‟ state.

* Resistor R is called a **Pull-up Resistor** because

it pulls the line voltage up to the high-voltage state when the switches are open.

# ENABLING & DISABLING INTERRUPTS

* All computers fundamentally should be able to enable and disable interruptions as desired.
* The problem of infinite loop occurs due to successive interruptions of active INTR signals.
* There are 3 mechanisms to solve problem of infinite loop:
  1. Processor should ignore the interrupts until execution of first instruction of the ISR.
  2. Processor should automatically disable interrupts before starting the execution of the ISR.
  3. Processor has a special INTR line for which the interrupt-handling circuit.

Interrupt-circuit responds only to leading edge of signal. Such line is called edge-triggered.

* Sequence of events involved in handling an interrupt-request:

1. The device raises an interrupt-request.
2. The processor interrupts the program currently being executed.
3. Interrupts are disabled by changing the control bits in the processor status register (PS).
4. The device is informed that its request has been recognized.

In response, the device deactivates the interrupt-request signal.

1. The action requested by the interrupt is performed by the interrupt-service routine.
2. Interrupts are enabled and execution of the interrupted program is resumed.

# HANDLING MULTIPLE DEVICES

* While handling multiple devices, the issues concerned are:

1. How can the processor recognize the device requesting an interrupt?
2. How can the processor obtain the starting address of the appropriate ISR?
3. Should a device be allowed to interrupt the processor while another interrupt is being serviced?
4. How should 2 or more simultaneous interrupt-requests be handled?

# POLLING

* Information needed to determine whether device is requesting interrupt is available in status-register
* Following condition-codes are used:
  + DIRQ  Interrupt-request for display.
  + KIRQ  Interrupt-request for keyboard.
  + KEN  keyboard enable.
  + DEN  Display Enable.
  + SIN, SOUT  status flags.
* For an input device, SIN status flag in used.

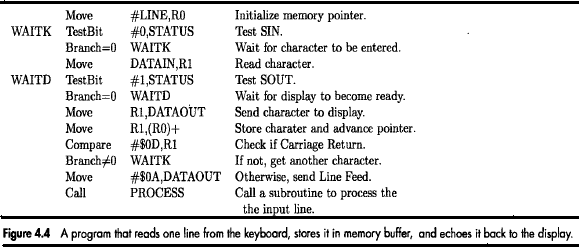
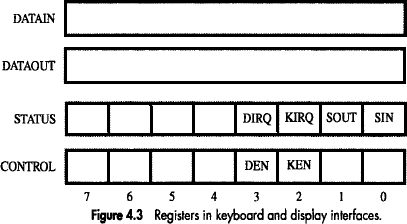
SIN = 1  when a character is entered at the keyboard.

SIN = 0  when the character is read by processor.

IRQ=1  when a device raises an interrupt-requests (Figure 4.3).

* Simplest way to identify interrupting-device is to have ISR poll all devices connected to bus.
* The first device encountered with its IRQ bit set is serviced.
* After servicing first device, next requests may be serviced.
* **Advantage:** Simple & easy to implement.

**Disadvantage:** More time spent polling IRQ bits of all devices.



# VECTORED INTERRUPTS

* A device requesting an interrupt identifies itself by sending a special-code to processor over bus.
* Then, the processor starts executing the ISR.
* The special-code indicates starting-address of ISR.
* The special-code length ranges from 4 to 8 bits.
* The location pointed to by the interrupting-device is used to store the staring address to ISR.
* The staring address to ISR is called the **interrupt vector**.
* Processor

→ loads interrupt-vector into PC &

→ executes appropriate ISR.

* When processor is ready to receive interrupt-vector code, it activates INTA line.
* Then, I/O-device responds by sending its interrupt-vector code & turning off the INTR signal.
* The interrupt vector also includes a new value for the Processor Status Register.

# CONTROLLING DEVICE REQUESTS

* Following condition-codes are used:
  + KEN  Keyboard Interrupt Enable.
  + DEN  Display Interrupt Enable.
  + KIRQ/DIRQ  Keyboard/Display unit requesting an interrupt.
* There are 2 independent methods for controlling interrupt-requests. (IE  interrupt-enable).

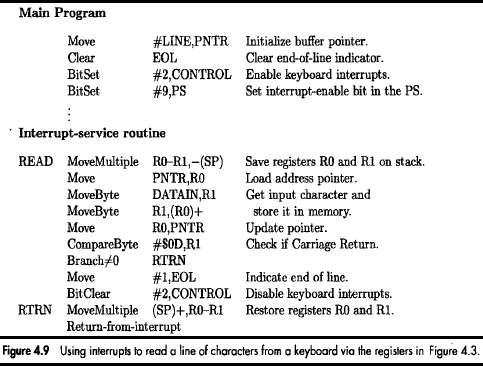
# At Device-end

IE bit in a control-register determines whether device is allowed to generate an interrupt-request.

1. **At Processor-end**, interrupt-request is determined by

→ IE bit in the PS register or

→ Priority structure



# INTERRUPT NESTING

* A multiple-priority scheme is implemented by using separate INTR & INTA lines for each device
* Each INTR line is assigned a different priority-level (Figure 4.7).
* Priority-level of processor is the priority of program that is currently being executed.
* Processor accepts interrupts only from devices that have higher-priority than its own.
* At the time of execution of ISR for some device, priority of processor is raised to that of the device.
* Thus, interrupts from devices at the same level of priority or lower are disabled.

# Privileged Instruction

* Processor's priority is encoded in a few bits of PS word. (PS  Processor-Status).
* Encoded-bits can be changed by **Privileged Instructions** that write into PS.
* Privileged-instructions can be executed only while processor is running in **Supervisor Mode**.
* Processor is in supervisor-mode only when executing operating-system routines.

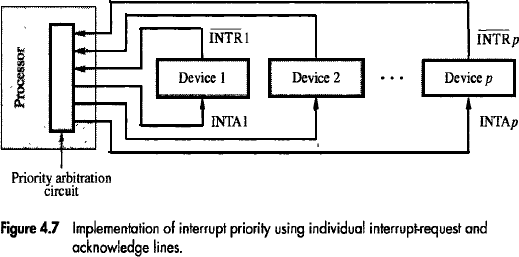
# Privileged Exception

* User program cannot

→ accidently or intentionally change the priority of the processor &

→ disrupt the system-operation.

* An attempt to execute a privileged-instruction while in user-mode leads to a **Privileged Exception**.



# SIMULTANEOUS REQUESTS

* The processor must have some mechanisms to decide which request to service when simultaneous requests arrive.
* INTR line is common to all devices (Figure 4.8a).
* INTA line is connected in a daisy-chain fashion.
* INTA signal propagates serially through devices.
* When several devices raise an interrupt-request, INTR line is activated.
* Processor responds by setting INTA line to 1. This signal is received by device 1.
* Device-1 passes signal on to device 2 only if it does not require any service.
* If device-1 has a pending-request for interrupt, the device-1

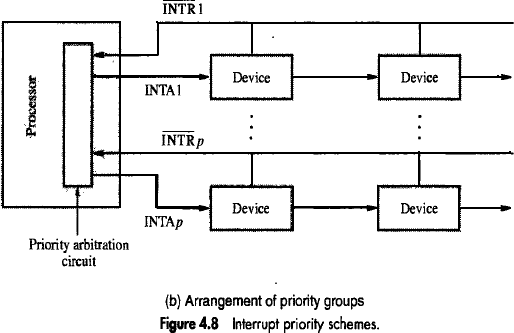
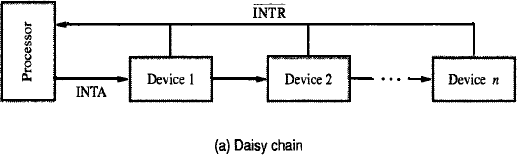
→ blocks INTA signal &

→ proceeds to put its identifying-code on data-lines.

* Device that is electrically closest to processor has highest priority.
* **Advantage:** It requires fewer wires than the individual connections.

# Arrangement of Priority Groups

* Here, the devices are organized in groups & each group is connected at a different priority level.
* Within a group, devices are connected in a daisy chain. (Figure 4.8b).



# DIRECT MEMORY ACCESS (DMA)

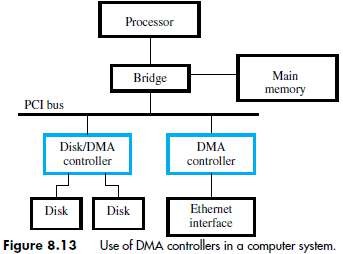
* The transfer of a block of data directly b/w an external device & main-memory w/o continuous involvement by processor is called DMA.
* DMA controller

→ is a control circuit that performs DMA transfers (Figure 8.13).

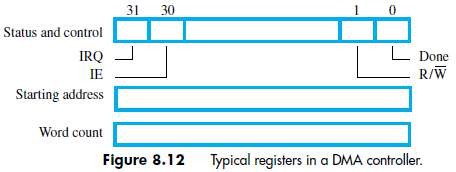
→ is a part of the I/O device interface.

→ performs the functions that would normally be carried out by processor.

* While a DMA transfer is taking place, the processor can be used to execute another program.



* DMA interface has three registers (Figure 8.12):
  1. First register is used for storing starting-address.
  2. Second register is used for storing word-count.
  3. Third register contains status- & control-flags.



* The R/W bit determines direction of transfer.

If R/W=1, controller performs a read-operation (i.e. it transfers data from memory to I/O), Otherwise, controller performs a write-operation (i.e. it transfers data from I/O to memory).

* If Done=1, the controller

→ has completed transferring a block of data and

→ is ready to receive another command. (IE  Interrupt Enable).

* If IE=1, controller raises an interrupt after it has completed transferring a block of data.
* If IRQ=1, controller requests an interrupt.
* Requests by DMA devices for using the bus are always given higher priority than processor requests.
* There are 2 ways in which the DMA operation can be carried out:

1. Processor originates most memory-access cycles.
   * DMA controller is said to "steal" memory cycles from processor.
   * Hence, this technique is usually called **Cycle Stealing***.*
2. DMA controller is given exclusive access to main-memory to transfer a block of data without any interruption. This is known as **Block Mode** (or burst mode).